# UNIVERSITY COLLEGE OF ENGINEERING
## OSMANIA UNIVERSITY, HYDERABAD
### M. E. (ECE, Mech. & CSE) I - Semesters (Main) Examination, March/April 2015
## MVSR ENGINEERING COLLEGE
## REVISED EXAMINATION TIME TABLE
### TIME : 2.00 PM TO 5.00 PM

| DATE & DAY | E. C. E. (EMBEDDED SYSTEMS & VLSI DESIGN) | MECHANICAL (CAD / CAM) | C. S. E. |
|---|---|---|---|
| | I-Semester | I-Semester | I-Semester |
| 23-03-2015 MONDAY | = = = = = | = = = = = | Advanced Algorithms |
| 25-03-2015 WEDNESDAY | Principles of VLSI System Design | = = = = = | Artificial Intelligence |
| 27-03-2015 FRIDAY | = = = = = | Computer Aided Modeling and Design | Data Mining |
| 30-03-2015 MONDAY | Micro Controllers for Embedded System Design | Computer Integrated Manufacturing | Advanced Operating Systems |
| 01-04-2015 WEDNESDAY | CPLD & FPGA Architectures and Applications | Finite Element Techniques | Object Oriented Software Engineering |
| 04-04-2015 SATURDAY | Digital IC Design | Experimental Techniques and Data Analysis | = = = = = |
| 06-04-2015 MONDAY | = = = = = | Vibration Analysis and Condition Monitoring | Mobile Computing |
| 08-04-2015 WEDNESDAY | **Data and Computer Communication Networks** | = = = = = | = = = = = |
| 10-04-2015 FRIDAY | Analog and Mixed Signal IC Design | Product Design and Process Planning | = = = = = |

DIRECTOR OF EVALUATION
EXAMINATION CELL